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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,075	03/23/2004	Michael J. Azevedo	SJO920030061US1	2651

46917 7590 02/25/2008
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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	PAPER NUMBER
2113	
MAIL DATE	DELIVERY MODE
02/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,075	AZEVEDO ET AL.	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29,32-34,41,44,46,53 and 57-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29,32-34,41,44,46,53 and 57-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is made **Non-Final**.

Claims 1-28,30,31,35-40,42,43,45,47-52, and 54-56 have been cancelled. Claims 29,32-34,41,44,46,53 and 57-63 have been examined. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 29,32-34,41,44,46,53 and 57-63 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 29, 41,53, and 60 recites the limitation "detecting an idle condition in said process interface before expiration of said timeout task" in lines 6-9 of claims and the limitation "forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires" on the last two lines of claim. If there is a detection of an idle condition, then the force performance of the error recovery instruction before an idle condition cannot occur. Only one of the two actions can occur at a time. Examiner suggest amending the limitation "detecting an idle condition in said processor interface before expiration of said timeout task; in response to said detection, withholding access to a local processor; performing the error recovery instruction while access to the local processor is withheld" to

"withholding access to a local processor and perform the error recovery instruction in response to detecting an idle condition in said processor interface before expiration of said timeout task".

The remaining claims, not specifically mentioned, are rejected because they are dependent upon one of the claims above.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 41,44,46, and 60-63 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claims 41,44,46, and 60-63, the claimed apparatus lacks hardware to enable the functionality. The claimed "logic"/"logic means" could be construed as software. As the claims lack hardware, they are not directed to physical "things". They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed software does not define any structural and functional interrelationships between the software and other claimed elements of a computer that permit the software functionality to be realized.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29,34,41,46,53,59-60 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,345,392 of Mito et al. referred hereinafter Mito in view of US Patent No. 6,543,002 of Kahle et al. referred hereinafter "Kahle".

In regards to claims 29,53, and 60 Mito discloses a method, apparatus, and program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction. Mito discloses receiving an interrupt (see figure 4 and column 8 lines 36-37).

monitoring a processor interface for an idle condition, detecting an idle condition in said processor interface before expiration of said timeout task. Mito discloses checking if I/O is active (see figure 4 item 192 and column 8 lines 40-45).

in response to said detection, withholding access to a local processor, and performing the error recovery instruction while access to the local processor is withheld. Mito discloses initiating a suspend routine (see column 8 lines 45-47).

However, Mito fails to disclose:

beginning a timeout task, and forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence. Kahle further discloses a hang condition is determined when the maximum

number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timeout task.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Mito and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating beginning a timeout task, and forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires. A person of ordinary skill in the art could have been motivated to combine the teachings because Mito is concerned with shutting down a system when there is a problem (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables shutting down a system when the problem is a hang condition (see column 6 lines 40-45).

In regards to claim 34,59, and 62, Mito in view of Kahle discloses the claim limitations as discussed above. Mito further discloses resuming normal operations after performing the error recovery instruction. Mito discloses a resume handler (see figure 7 and column 9 lines 15-27)

In regards to claim 41, Mito discloses an apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic for receiving an error recovery instruction. Mito discloses receiving an interrupt (see figure 4 and column 8 lines 36-37).

wherein the self-quiesce logic begins to monitor a processor interface for an idle condition, detects an idle condition in said processor interface. Mito discloses checking if I/O is active (see figure 4 item 192 and column 8 lines 40-45).

in response to said detection, withholds access to a local processor, performs the error recovery instruction while access to the processor is withheld Mito discloses initiating a suspend routine (see column 8 lines 45-47).

However, Mito fails to explicitly disclose

a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction, wherein the self-quience logic initiates the timer when the error recovery instruction is received, and forces performance of the recovery of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence. Kahle further discloses a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timeout task.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Mito and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction, wherein the self-quience logic initiates the timer when the error recovery instruction is received, and forces performance

of the recovery of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires. A person of ordinary skill in the art could have been motivated to combine the teachings because Mito is concerned with shutting down a system when there is a problem (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables shutting down a system when the problem is a hang condition (see column 6 lines 40-45).

In regards to claim 46, Mito in view of Kahle discloses the claim limitations as discussed above. Mito further discloses wherein the self-quiesce logic allows resuming normal operations after performing the error recovery instruction. Mito discloses a resume handler (see figure 7 and column 9 lines 15-27).

Claim 29,32-34,41,44,46,53 and 57-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,974,147 of Hanrahan et al. referred hereinafter "Hanrahan" in view of Kahle.

In regards to claim 29,53, and 60, Hanrahan discloses a method, apparatus, and program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

monitoring a processor interface for an idle condition. Hanrahan discloses determining when there are no longer bus requests (see column 7 lines 20-23)

detecting an idle condition in said processor interface before expiration of said timeout task, and in response to said detection, withholding access to a local processor. Hanrahan discloses performing no further activity (see column 7 lines 20-23)

performing the error recovery instruction while access to the local processor is withheld Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to disclose:

beginning a timeout task, and forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence. Kahle further discloses a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45), indicating a timeout task.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded, thus indicating a timeout task, and forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires. A person of ordinary skill in the art could have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see

column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 32,57,and 61, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses

withholding access to the processor interface when the idle condition is detected. Hanrahan discloses performing no further activity (see column 7 lines 20-23).

after access to the processor interface is withheld, interrogating data transfer paths in the processor interface to determine when the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

performing the error recovery instruction when the data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 33,34,58,59,62, and 63 Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses resuming normal operations after performing the error recovery instruction. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

In regards to claim 41, Hanrahan discloses an apparatus for use with a local processor and forquiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic for receiving an error recovery instruction. Hanrahan discloses a receiving a quiesce signal (see column 9 line 13-14).

wherein the self-quiesce logic begins to monitor a processor interface for an idle condition. Hanrahan discloses determining when there are no longer bus requests (see column 7 lines 20-23).

detects an idle condition in said processor interface before expiration of said timer, in response to said detection, withholds access to a local processor. Hanrahan discloses performing no further activity (see column 7 lines 20-23).

performs the error recovery instruction while access to the local processor is withheld. Hanrahan discloses sequencing to a known state for retry, recover, and debug operations (see column 2 lines 24-26).

However, Hanrahan fails to explicitly disclose:

a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction, wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, and forces performance of the recovery of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires.

Kahle disclose a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of completion valid signal is exceeded (see column 6 lines 40-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hanrahan and Kahle to have a hang detection unit for recovering from a hang condition via a hang recovery sequence, wherein a hang condition is determined when the maximum number of clock cycles since the most recent assertion of

completion valid signal is exceeded, thus indicating a timer for determining when to force execution of the error recovery instruction, wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, and forces performance of the recovery of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires. A person of ordinary skill in the art could have been motivated to combine the teachings because Hanrahan is concerned with recovering from system errors (see column 1 lines 23-25), and incorporating a hang detection unit, as per teachings of Kahle, enables recovery from errors resulting from hang conditions (see column 6 lines 40-45).

In regards to claim 44, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses

wherein the self-quiesce logic withholds access to the local processor. Hanrahan discloses determining when there are no longer bus requests (see column 7 lines 20-23).

withholding access to the processor interface when the idle condition is detected. Hanrahan discloses performing no further activity (see column 7 lines 20-23).

after access to the processor interface is withheld, interrogates data transfer paths to determine when the data paths are idle. Hanrahan discloses waiting for all operations to complete before sequencing to a known state (see column 9 lines 15-20).

performing the instruction by performing the error recovery instruction when the data transfer paths are idle. Hanrahan discloses sequencing to a known state when all current operations that have completed (see column 9 lines 15-22).

In regards to claim 46, Hanrahan in view of Kahle discloses the claim limitations as discussed above. Hanrahan further discloses wherein the self-quiesce logic allows resuming

normal operations after the error recovery instruction is performed. Hanrahan discloses resuming operations following the quiesce state (see column 9 lines 24-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is 571-272-3652. The examiner can normally be reached on 9-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Emerson C Puente/
Primary Examiner, Art Unit 2113